

# Notice of Allowability

Application No.

10/715,524

Examiner

Ly D Pham

Applicant(s)

ASHIKAGA, KINYA

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 14 October 2004.
2. ☒ The allowed claim(s) is/are 7-18.
3. ☒ The drawings filed on 19 November 2003 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☒ All   b) ☐ Some\*   c) ☐ None   of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☒ Certified copies of the priority documents have been received in Application No. 09/943,513.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

## Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

  
David Nelms  
Supervisory Patent Examiner  
Technology Center 2800

### DETAILED ACTION

1. Applicant's Amendment filed October 14, 2004 has been entered. Claims 1 – 6 have been cancelled. Claims 7 – 9 have been amended. New claims 12 – 18 have been added.

### *Allowable Subject Matter*

2. Claims 7 – 18 are allowed.

3. The following is an examiner's statement of reasons for allowance:

The prior art (exemplary US Pat 5,022,009) teaches a semiconductor memory comprising:

first, second, and third bit lines;

a first memory cell connected to either the first bit line or the second bit line;

a first dummy memory cell connected to either the second bit line or the third bit line;

a second dummy memory cell connected to either the third bit line or the fourth bit line;

wherein when a memory cell connected to the first bit line is selected, the second dummy cell is simultaneously selected, and the first bit line is connected to a first terminal of the sense amplifier, and the third bit line and the fourth bit line are connected

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to a second terminal of the sense amplifier, and then potentials of the first and second terminals are sense amplified; and

wherein when a memory cell connected to the third bit line is selected, the first dummy cell is simultaneously selected, the third bit line is connected to the second terminal of the sense amplifier, and the first bit line and the second bit line are connected to the first terminal of the sense amplifier, and then the potentials of the first and second terminals are sense amplified.

However, the prior art did not teach the semiconductor memory, further comprising:

the first memory cell which induces a first electric potential onto the first bit line;

the first dummy memory cell having a ferroelectric capacitor polarized to a first direction and inducing a second electric potential onto the second bit line;

the second dummy memory cell having a ferroelectric capacitor polarized to a second direction opposite to the first direction and inducing a third electric potential onto the third bit line;

a short-circuiting device which shorts the second and third bit lines;

a sense amplifier which compares an electric potential of the first bit line with an electric potential of the second bit line and outputs an amplified voltage to each of the first and second bit lines in accordance with a result of the comparison.


4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.  
  
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham   
November 23, 2004

  
David Nelms  
Supervisory Patent Examiner  
Technology Center 2800